Listing of Claims

This listing of claims replaces all prior versions and listings of claims in the application.

1. (Previously presented) A system for generating amplitude matched, phase shifted signals, comprising:

a filter arrangement including a plurality of input and output nodes, a first set of input nodes arranged to receive an input signal, a second set of input nodes coupled to electrical ground, each output node configured to provide an associated vector that is offset in phase from a vector associated with each other output node;

a first peak detector arranged to receive a first pair of vectors from corresponding output nodes of the filter arrangement that are approximately 180° different in phase from each other, the first peak detector configured to generate a first peak signal;

a second peak detector arranged to receive a second pair of vectors from corresponding output nodes of the filter arrangement that are approximately 180° different in phase from each other and different from the first pair of vectors, the second peak detector configured to generate a second peak signal;

a comparator arranged to receive the first peak signal and the second peak signal and generate a feedback signal;

an adjustable element associated with each output node, the adjustable element configured to receive the feedback signal and in response to the feedback signal substantially equalize an amplitude of each vector associated with each output node;

an adder element arranged to receive the first pair of vectors and the second pair of vectors and configured to add respective vectors from the first and second pair of vectors each shifted in phase by approximately 90° from the other vector to generate corresponding adder outputs shifted in phase from the phase of the respective vectors from the first and second pair of vectors; and

a scaler configured to receive the vectors associated with each output node and attenuate the amplitude of each of the same to generate a set of scaler outputs that are substantially equal in magnitude to the adder outputs.

2. (Previously presented) The system of claim 1, wherein four output nodes are associated with the filter arrangement, each output node having an associated vector.

3. (Previously presented) The system of claim 2, wherein the adder element is configured to add the four vectors resulting in eight phase shifted vectors.

4. (Previously presented) The system of claim 3, wherein the scaler is configured to scale the amplitude of the four vectors resulting in eight amplitude matched phase shifted vectors.

5. (Original) The system of claim 4, wherein the adjustable element is an adjustable resistance.

6. (Original) The system of claim 5, wherein the adjustable resistance is a metal oxide semiconductor field effect transistor (MOSFET) adjustable resistance.

7. (Original) The system of claim 4, wherein the adjustable element is an adjustable capacitance.

8. (Original) The system of claim 7, wherein the adjustable capacitance is a varactor.

9. (Previously presented) A method for generating amplitude matched, phase shifted signals, comprising:

providing a plurality of vectors, each vector associated with a respective output node, each vector offset in phase from each other vector associated with each other output node;

applying an input signal at a subset of a set of input nodes;

generating a first peak signal responsive to a first pair of vectors that are approximately 180° different in phase from each other;

generating a second peak signal responsive to a second pair of vectors different from the first pair of vectors, the second pair of vectors approximately 180° different in phase from each other;

generating a feedback signal responsive to the first peak signal and the second peak signal;

providing the feedback signal to a respective adjustable element associated with each input and output node;

adjusting each adjustable element using the feedback signal to substantially equalize an amplitude of each vector associated with each output node; and

applying each vector to an adder element and to a scaler, wherein an output of the adder element is substantially equal in amplitude to an output of the scaler.

10. (Previously presented) The method of claim 9, wherein the feedback signal is applied to a resistance to substantially equalize an amplitude of each vector associated with each output node.

11. (Previously presented) The method of claim 9, wherein the feedback signal is applied to a capacitance to substantially equalize an amplitude of each vector associated with each output node.

12. (Original) The method of claim 10, further comprising adjusting the resistance using a metal oxide semiconductor field effect transistor (MOSFET) adjustable resistance.

13.-14. (Canceled)

15. (Original) The method of claim 11, further comprising adjusting the capacitance using a varactor.

16.-17. (Canceled)

18. (Previously presented) A system for generating amplitude matched, phase shifted signals, comprising:

filter means including a plurality of input and output nodes, a first set of input nodes arranged to receive an input signal, a second set of input nodes coupled to electrical ground, the filter means for providing a plurality of associated vectors that are offset in phase from each other vector associated with each other output node;

means for generating a first peak signal responsive to a first pair of vectors that are approximately 180° different in phase from each other;

means for generating a second peak signal responsive to a second pair of vectors different from the first pair of vectors, the second pair of vectors approximately 180° different in phase from each other;

means for generating a feedback signal responsive to the first peak signal and the second peak signal;

means for providing the feedback signal to an adjustable element associated with each output node;

means for using the feedback signal to substantially equalize an amplitude of each vector associated with each output node;

means for applying each vector to an adder element; and

means for applying each vector to a scaler, wherein an output of the adder element is substantially equal in amplitude to an output of the scaler.

19. (Original) The system of claim 18, wherein the means for substantially equalizing an amplitude of each vector comprises adjustable resistance means.

20. (Original) The system of claim 18, wherein the means for substantially equalizing an amplitude of each vector comprises adjustable capacitance means.

21. (Original) The system of claim 19, wherein the adjustable resistance means comprises a metal oxide semiconductor field effect transistor (MOSFET) adjustable resistance.

22.-23. (Canceled)

24. (Previously presented) A system for generating amplitude matched, phase shifted signals, in a portable communication device, comprising:

a portable communication device including a transmitter and a receiver;

a synthesizer for providing a local oscillator signal;

a filter arrangement configured to operate on the local oscillator signal, the filter arrangement including a plurality of input and output nodes, a first set of input nodes arranged to receive the local oscillator signal, a second set of input nodes coupled to electrical ground, each output node configured to provide an associated vector that is offset in phase from a vector associated with each other output node;

a first peak detector arranged to receive a first pair of vectors from corresponding output nodes of the filter arrangement that are approximately 180° different in phase from each other, the first peak detector configured to generate a first peak signal;

a second peak detector arranged to receive a second pair of vectors from corresponding output nodes of the filter arrangement that are approximately 180° different in phase from each other and different from the first pair of vectors, the second peak detector configured to generate a second peak signal;

a comparator arranged to receive the first peak signal and the second peak signal and generate a feedback signal;

an adjustable element associated with each output node, the adjustable element configured to receive the feedback signal and in response to the feedback signal substantially equalize an amplitude of each vector associated with each output node;

an adder element arranged to receive the first pair of vectors and the second pair of vectors and configured to add respective vectors from the first and second pair of vectors wherein each respective vector is shifted in phase from the other to generate respective adder outputs shifted in phase from the phase of the first pair of vectors and the second pair of vectors; and

a scaler configured to receive the vectors associated with each output node and attenuate the amplitude of each of the same to generate a set of scaler outputs that are substantially equal in

magnitude to the adder outputs.

25. (Previously presented) The system of claim 24, wherein four output nodes are associated with the filter arrangement, each output node having an associated vector.

26.-27. (Canceled)

28. (Previously presented) The system of claim 24, wherein the adjustable element is an adjustable resistance.

29. (Original) The system of claim 28, wherein the adjustable resistance is a metal oxide semiconductor field effect transistor (MOSFET) adjustable resistance.

30. (Previously presented) The system of claim 24, wherein the adjustable element is an adjustable capacitance.

31. (Original) The system of claim 30, wherein the adjustable capacitance is a varactor.